

Miniaturized electronic system for the planetary integrated camera spectrometer

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ABSTRACT

This paper discusses the design and implementation of a miniaturized electronic system for the Planetary Integrated Camera-Spectrometer (PICS). The PICS electronics demonstrates the application of Field Programmable Gate Arrays (FPGAs) and of analog hybrid technology to space flight multi-spectral systems. A discussion of the electronic system design illustrates how a multi-sensor instrument consisting of an UV CCD, two visible CCDs, and a near-IR focal plane assembly can be processed through a common set of electronics. Following the system design discussion, the actual electronic design will be presented. Each miniaturized module will be discussed as to functionality and performance. The test setup for bench checkout of a cooled CCD and an IR FPA, including results with bead electronics and with the hybrids are also described.

1. INTRODUCTION

The Planetary Integrated Camera-Spectrometer (PICS)¹ will collect images for mineralogical mapping and atmospheric composition studies over a wide spectral range of planetary systems. PICS will also conduct experiments in solar occultation by the atmosphere of a planet. The PICS instrument is composed of four channels: an UV channel covering 160 spectral channels (70-150 nm), a dual-CCD visible imaging system (simultaneously shuttered in two colors 300-500 nm and 500-1000 nm), and a near-IR channel covering from 1300 to 2600 nm with a spectral resolution of 5 nm.

2. INSTRUMENT APPROACH

The new generation of small planetary instruments shall conform to mass and power limitations caused by budgetary constraints coupled with the lack of heavy launch vehicles; combining instrument functions along with innovation in electronics design and packaging will conserve limited spacecraft resources.

The PICS instrument approach is to maximize the commonality between the different channels; for example, the visible CCDs and IR detectors share a single lightweight, multi-wavelength, off-axis Gregorian telescope and are mounted directly on a single radiator. Also, the four channels of the integrated camera spectrometer share one signal processing electronics which is fabricated in a hybrid module, the clock drivers and bias for each CCD channel and for the IR FPA are also provided by dedicated hybrid modules. The digital control and timing for all four channels is generated using a single field programmable gate array (FPGA).

The test setup for bench checkout of the PICS detector-electronics shown in Figure 1, consists of CCD and IR detectors, instrument electronics, a computer interface box, and a PC 486 computer with customized software.

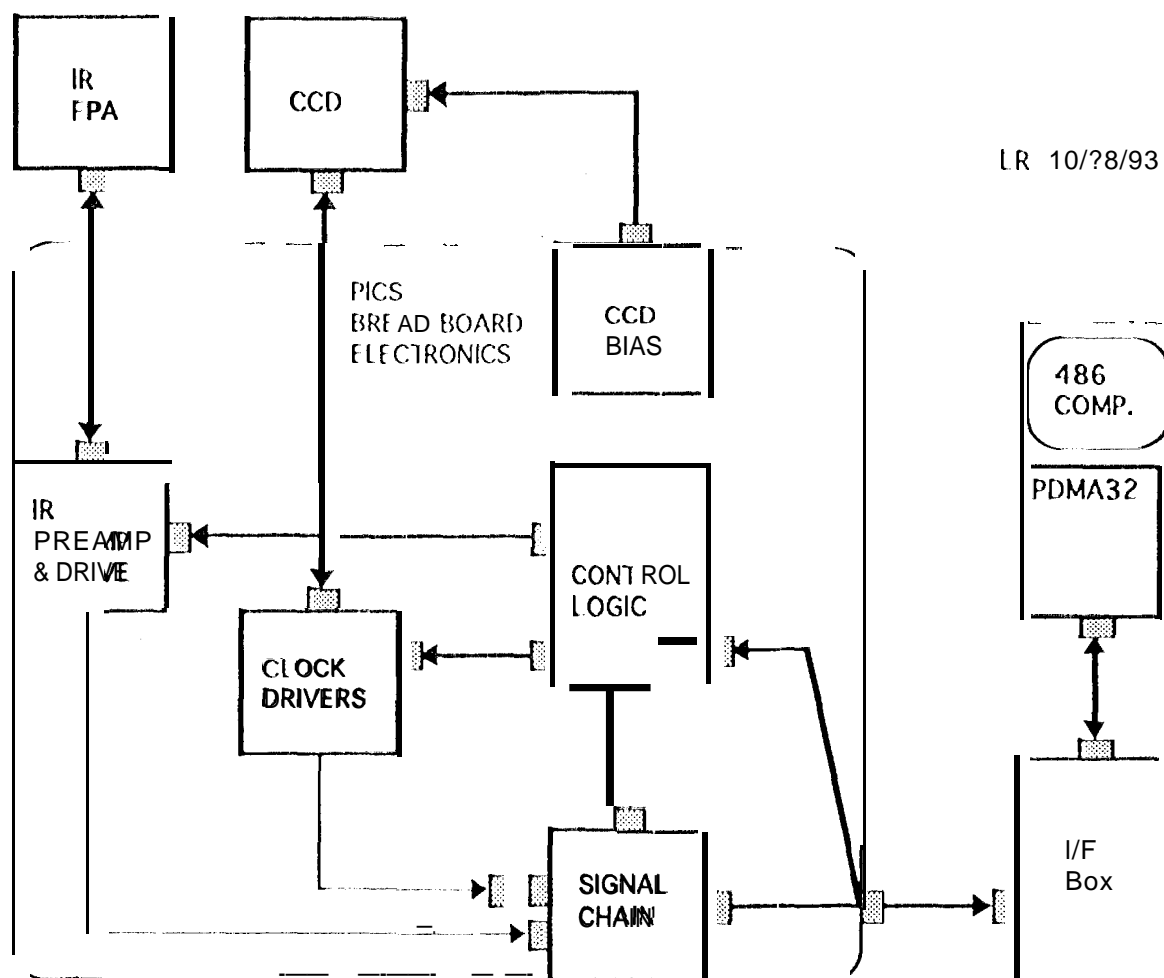


Figure 1. PICS detector-electronics test Setup.

2. DETECTORS

The Short Wave Infrared (SWIR) channel of PICS is based on a 256 by 256 Mercury Cadmium Telluride (HgCdTe) photovoltaic diode array multiplexed (via Indium bump bonds) into four independent quadrants using (Near IR Camera and Multi-Object Spectrograph (NICMOS III))^{2,3} multiplexers fabricated by Rockwell international Science Center. The IR FPA consists of a source-follower per detector (SFD) configuration and a common output amplifier.

The visible channel for PICS is based on two front-side illuminated CCDs fabricated by Loral, each CCD is made of 1024 by 2048 elements. The CCD optimized for detection in the blue is lumigen coated.

A CCD mounted on an image intensifier for the UV channel is of the same type as that used in the visible channel to simplify data acquisition and control electronics, it is constructed by the University of Arizona, supported by the Johns Hopkins University Applied Physics Laboratory. The intensifier consists of a single, microchannel plate (MCP) for electron multiplication with a phosphor output to convert the electron pulse into photons which are then recorded with the CCD.

3. ELECTRONICS SYSTEM

Each CCD detector including the UV-CCD, is interfaced with a dedicated Clock Drive/Bias hybrid module; these hybrid modules provide the regulated bias voltages and clocks (level translation for serial and parallel registers) necessary to operate the CCD detectors. Included in this Clock Drive/Bias hybrid module is a high speed/low-noise preamplifier stage which provides offset and gain prior to further signal processing. The IR Clock Drive/Bias hybrid module also contains a preamplifier stage and a clamping circuit for removing the pedestal which results from the over clocking mode in which the FPA is operated. These hybrid modules are placed in close proximity with their respective detectors to minimize noise and EMI interference.

The preamplified signals from all four detectors are multiplexed into one signal chain fabricated in a hybrid module. The signal chain consists of an amplifier, a double-pole filter, and a buffer amplifier with offset control that feeds the signal from the selected channel into a low power 8-bit flash A/D converter (the A/D converter is not included in a hybrid). This signal chain hybrid module, has the capability of subtracting a VIDEO signal from a REF signal, or just straight VIDEO signal sampling. Only 8 bits digitization are needed to reduce data transfer size at the selected readout rate of 300 Kpixels/sec.

Detector timing for all four channels, are generated by an Actel FPGA which is interfaced to an I/O board for data/commands transfer to and from the computer. The IR FPA is operated by resetting the array and sampling the pedestal level of each detector after the reset pulse has been released; then, after integration, the integrated signal is sampled; finally after digitization the pedestal level is subtracted from the integrated signal level for each pixel of the IR FPA.

Integration time (exposure time) for all four channels is commanded from the computer which performs image display, engineering evaluation and statistical analysis on data from the selected channel.

The noise performance of the CCD detectors has been measured at 16 electrons rms using the breadboard electronics, and with no change with the FPGA and hybrid modules. Preliminary IR channel tests have been done with the NICMOS-3 multiplexer only (that is no HgCdTe array) at 300 Kpixels/sec and at a temperature of 75 K both with breadboard electronics and with the FPGA and hybrid modules.

The total power consumption of the signal processing electronics hybrid modules and the FPGA, including the A/D converter is about 450 mW, with a total estimated mass of 370 grams including the PCB boards.

The PICS modes of operation are:

1. Idle, in which the cameras are not taking or reading exposure.
2. Take, all or any number of detectors may be exposed
3. Read, reads data from a selected detector.
(multiple channel readouts are done sequentially)
4. Area array /frame transfer clocking.
5. Detector flush.
6. 2x2 Pixel summing
7. Window. readout of area of interest

Future activities include integration and evaluation of all four channels with the optics and with the radiator. Figure 2 shows a picture of the hybrid modules and the FPGA, and figure 3 is a sample picture taken with the CCD channel

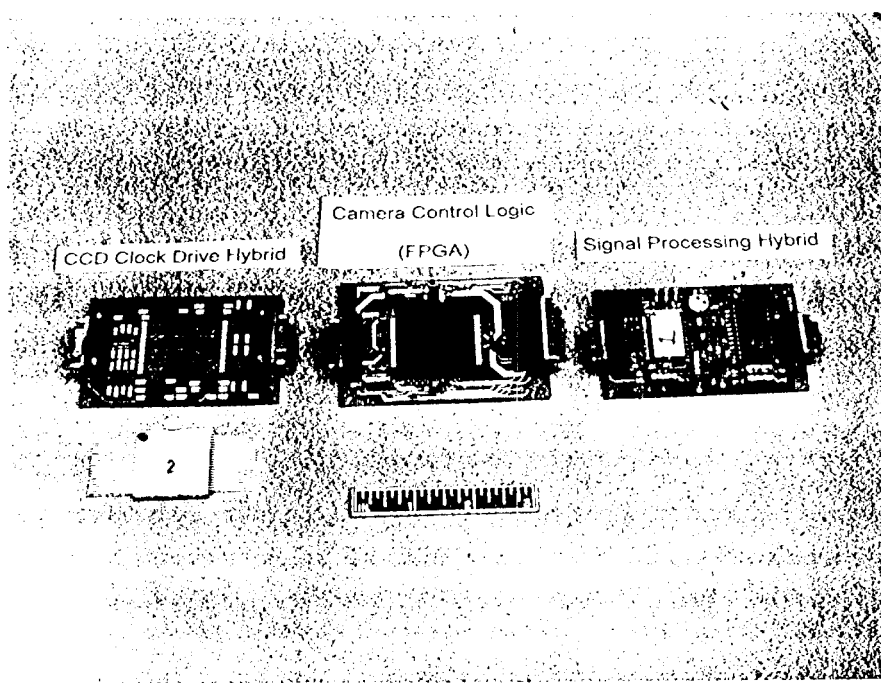


Fig. 3. PICS hybrid modules and FPGA.

Image A Image A.B Palette Functions

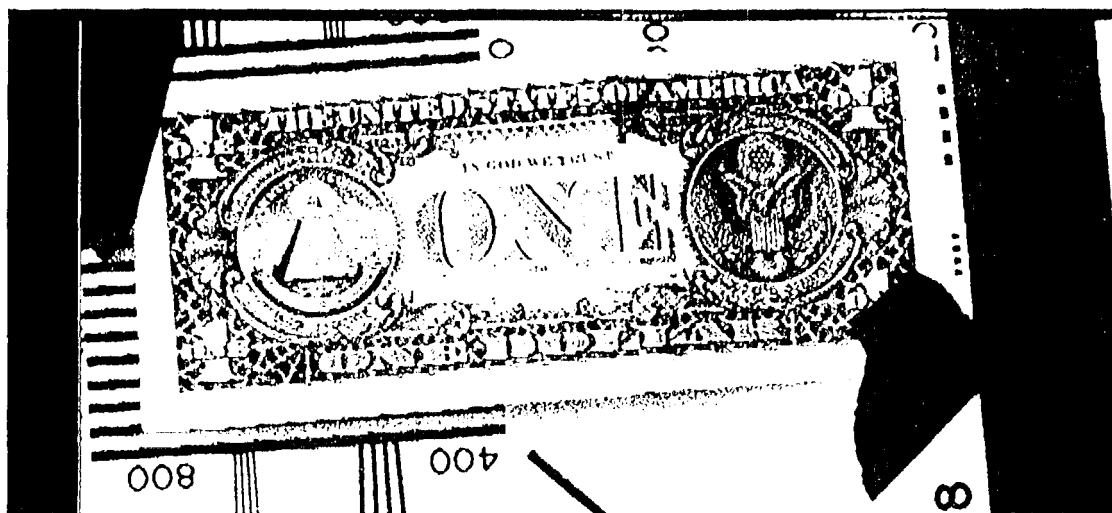


Figure 4. Sample picture with CCD

5. ACKNOWLEDGMENTS

The authors are grateful to George Frachetti and Pat Beauchamp for their support, and to Charlie Davis, Johnny Johnston and Carolina Flores-Helizon for their technical assistance. The activities described in this paper were performed by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration,

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